CLAIMS

What is claimed is:

1. A memory device, comprising:

a plurality of device circuitry coupled to a plurality of device pads;

an operation interface to operate the memory device in an operation mode;

a plurality of interfaces to operate the memory device in a plurality of other modes, each interface of the plurality of interfaces having a predetermined correlation between the plurality of device circuitry and the plurality of device pads; and

a configuration circuit to select among the operation interface and the plurality of interfaces.

2. The memory device of claim 1, wherein the operation interface has a third set of address pads and wherein the plurality of interfaces comprises:

a test interface to test the memory device for defects, the test interface having a first set of address pads; and

a programming interface to program the memory device with a code, the programming interface having a second set of address pads.

3. The memory device of claim 2, wherein the first set of address pads enables parallel addressing of the memory device in one cycle.

4. The memory device of claim 3, wherein the test interface is a standard flash memory interface.

5. The memory device of claim 2, wherein the second set of address pads of the programming interface has fewer address pads than the first set of address pads of the test interface.

6. The memory device of claim 2, wherein the third set of address pads of the operation interface are multiplexed address and data pads.

7. The memory device of claim 6, wherein the operation interface is a proprietary interface.

8. The memory device of claim 1, wherein the configuration circuit comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

9. The memory device of claim 8, wherein the operation interface has a third set of address pads and wherein the plurality of interfaces comprises:

a test interface to test the memory device for defects, the test interface having a first set of address pads; and

a programming interface to program the memory device with a code, the programming interface having a second set of address pads.

10. A component board, comprising:

a processor; and

a memory coupled to the processor, the memory comprising:

a plurality of device circuitry coupled to a plurality of device pads;

an operation interface to operate the memory in an operation mode;

a plurality of interfaces to operate the memory in a plurality of other modes, each interface of the plurality of interfaces having a predetermined correlation between the plurality of device circuitry and the plurality of device pads; and

a configuration circuit to select among the operation interface and the plurality of interfaces.

11. The component board of claim 10, wherein the configuration circuit comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

12. The component board of claim 11, wherein the plurality of interfaces comprises:

a test interface to test the memory; and

a programming interface to program the memory with a code.

13. The component board of claim 12, wherein the BIOS memory is a flash memory.

14. The component board of claim 13, wherein the test interface is a standard flash interface and wherein the operation interface is a proprietary interface.

15. A computer system, comprising:

a peripheral device; and

a system board coupled to the peripheral device, the system board comprising:

a processor; and

a memory coupled to the processor, the memory comprising:

a plurality of device circuitry coupled to a plurality of device pads;

an operation interface to operate the memory in the computer system;

a plurality of interfaces to operate the memory in a plurality of modes, each interface of the plurality of interfaces having a predetermined correlation between the plurality of device circuitry and the plurality of device pads; and

a configuration circuit to select among the operation interface and the plurality of interfaces.

16. The computer system of claim 15, wherein the plurality of interfaces comprises:

a test interface to test the memory; and

a programming interface to program the memory.

17. The computer system of claim 16, wherein the BIOS memory is a flash memory.

18. The computer system of claim 17, wherein the test interface is a standard flash interface and wherein the operation interface is a proprietary interface.

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